FIG. 1

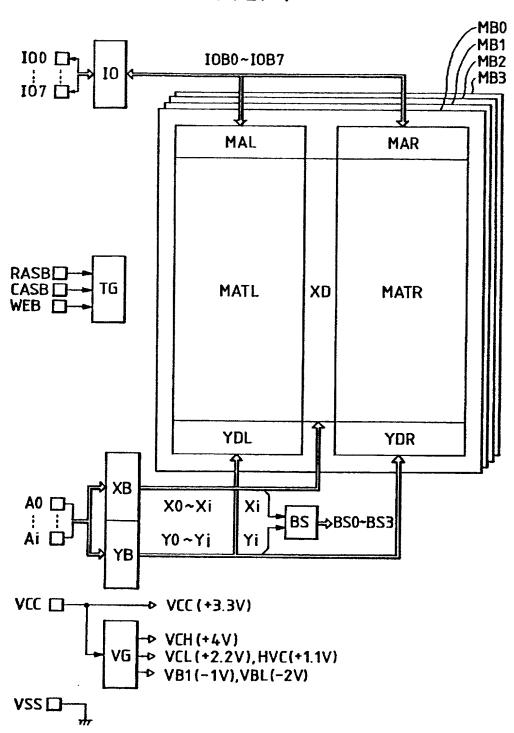
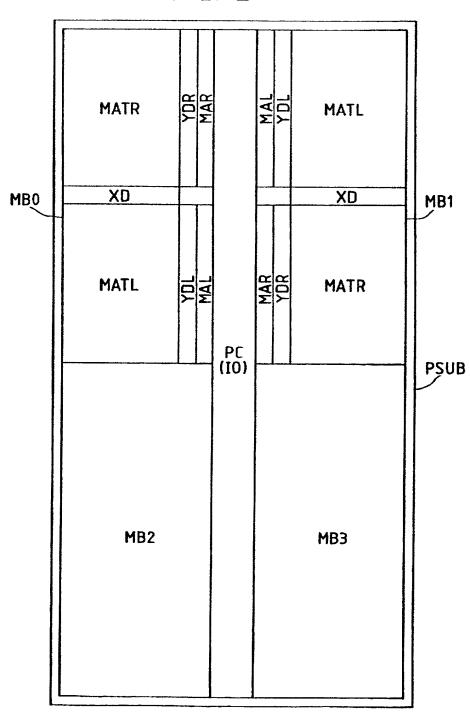
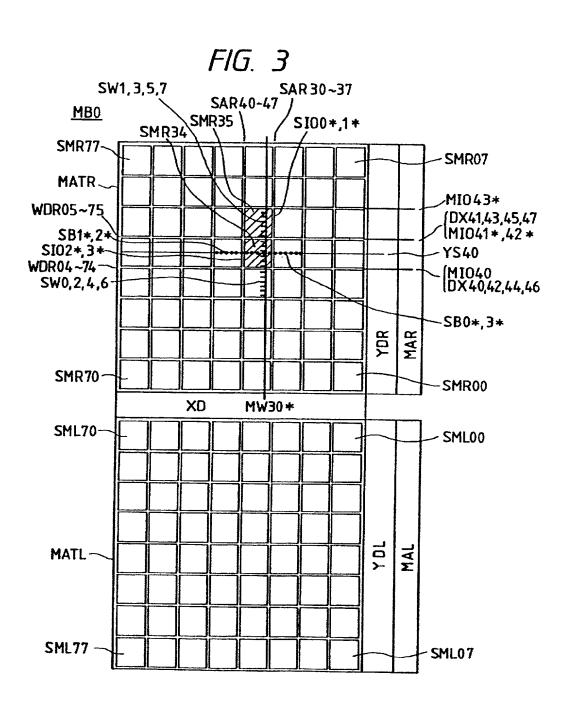


FIG. 2





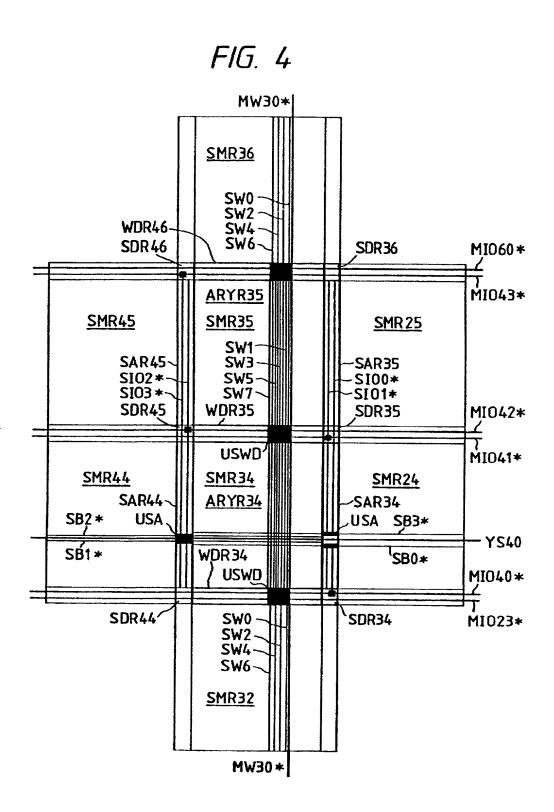


FIG. 5 SI02* *0EWM **SI00*** \$103****** SW7 SW5 SW3 SW1 存 SI01* 夺 **⇔MIO42*** DX41, 43,45,47 US US US US WD WD WDR35 SDR45-SDR35 #MI041* SB254* USA **USA** -**\$**SB255* **∀YS463** SB253 * USA USA **⇔**SB252* SAR44~ ARYR34 SAR34 USA USA **#**SB3* SB2 * 4 SB1 * #-USA **USA ⇔**SB0* **⇔**MI040* SH4R[△] ^SH3L DX40, US us us us k WD WD WD WD 42,44,46 SH4L, SDR44 SDR34 SH3R WDR34 **#MI023*** *£01S SMR34 SW6 SW4 SW2 SWO MW30*

#: MEMORY CELL 中, 中: SWITCH

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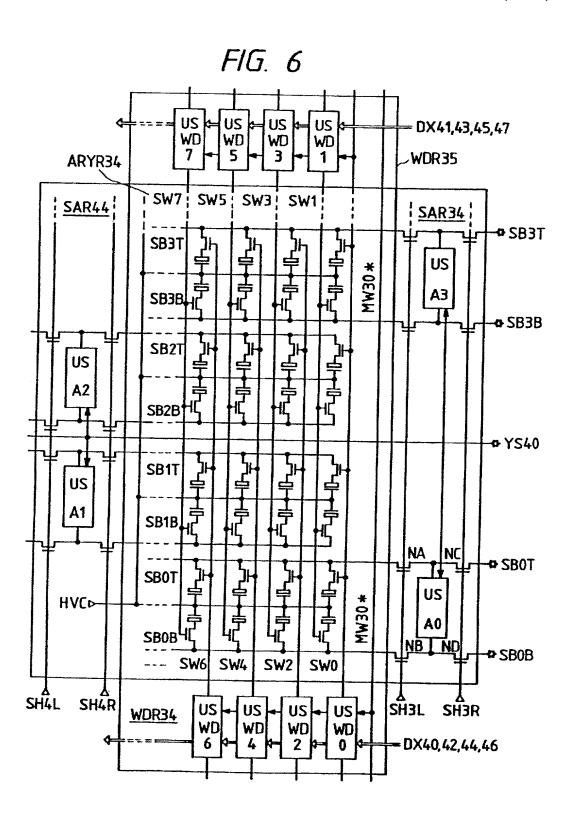
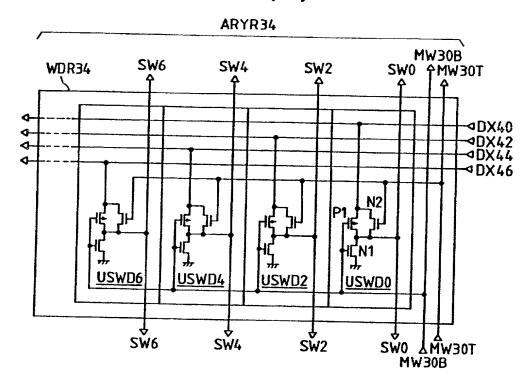


FIG. 7(A)



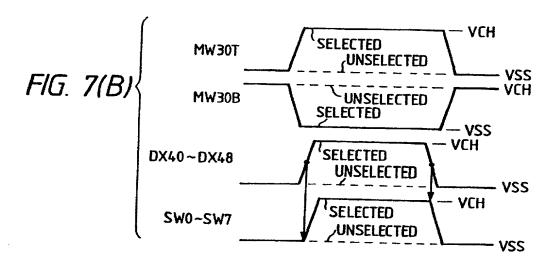
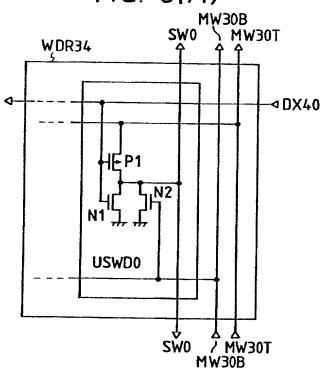




FIG. 8(A)



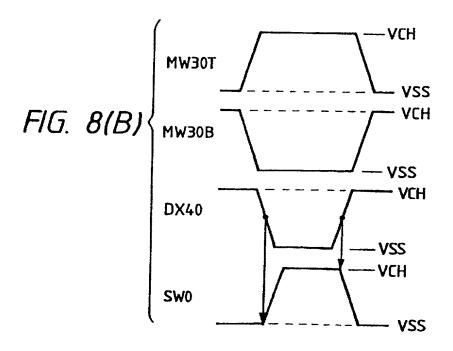
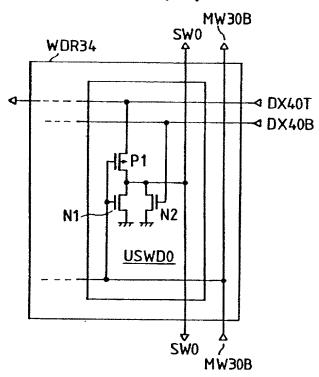
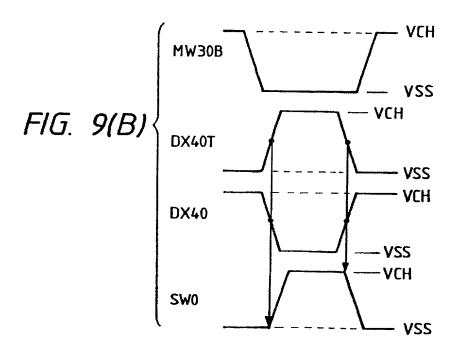
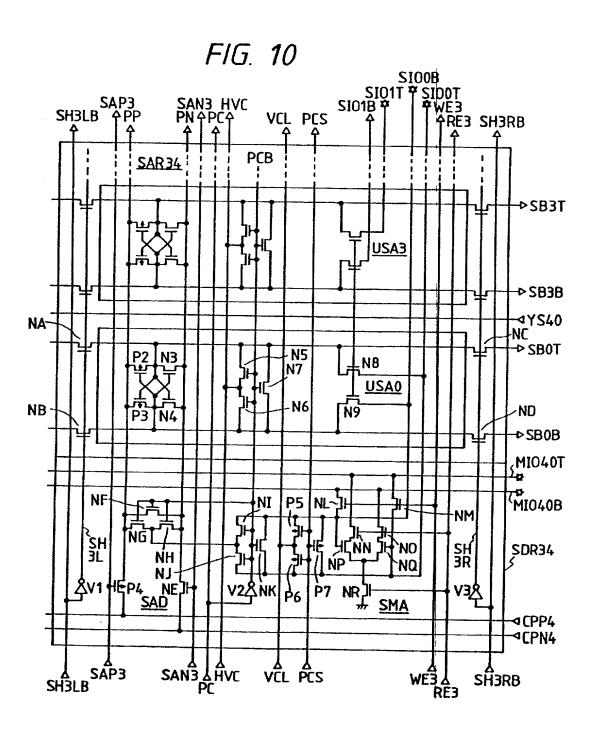
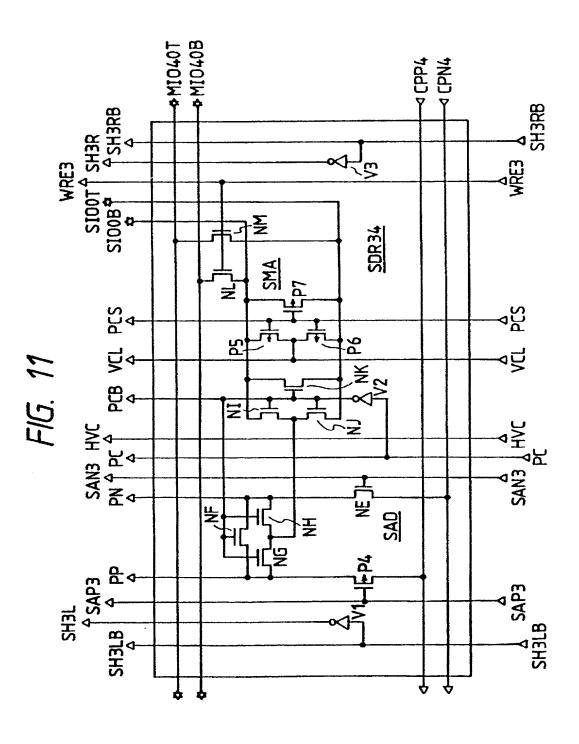


FIG. 9(A)









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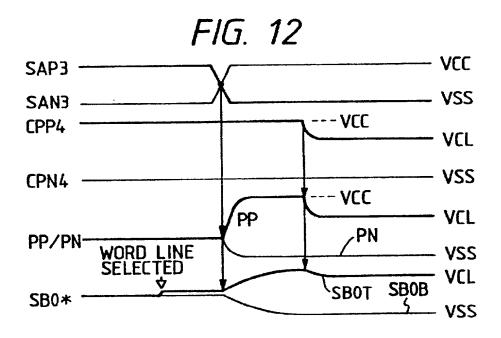


FIG. 14 **VCC SAP31** -VSS SAN3 SAP32 -VCC **VSS** -- VCC PP VCL PN PP/PN WORD LINE SELECTED VSS VCL SB0B SBOT SB0* - VSS

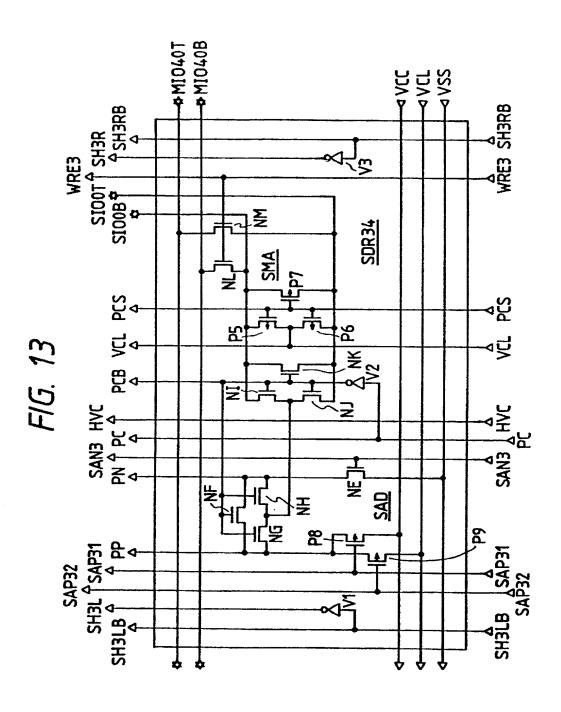


FIG. 15

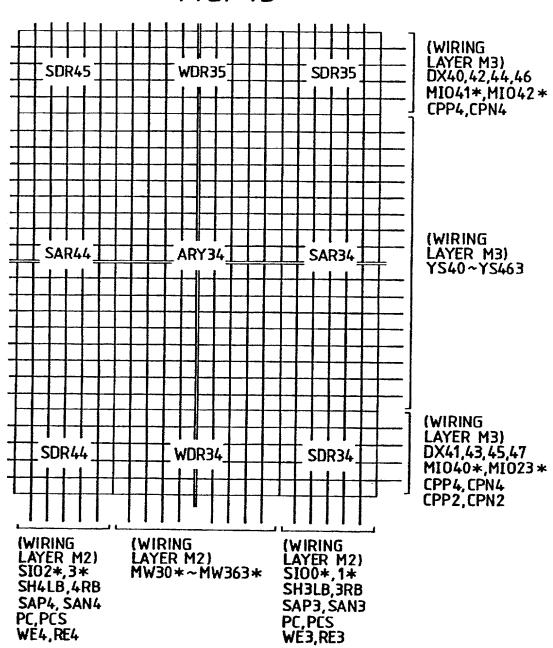


FIG. 16

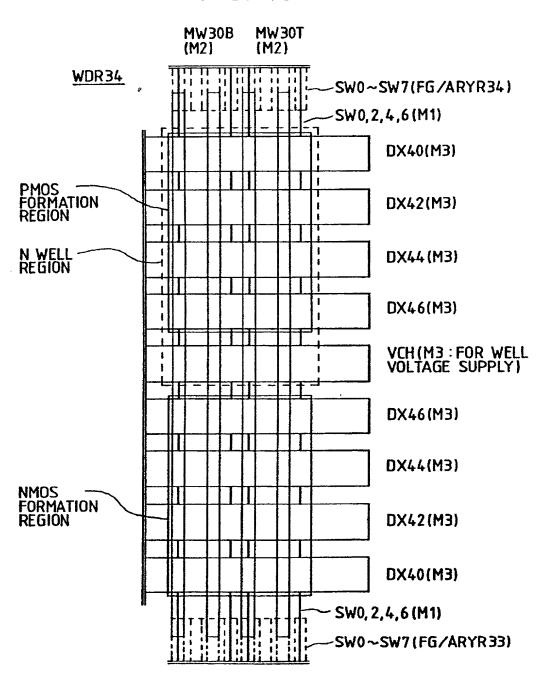
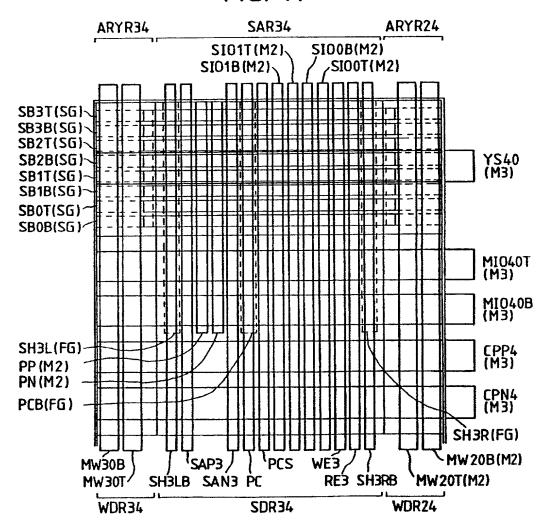
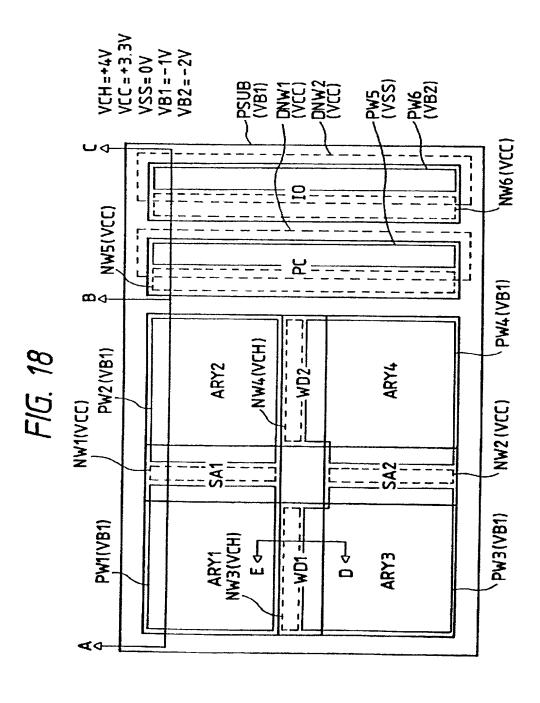
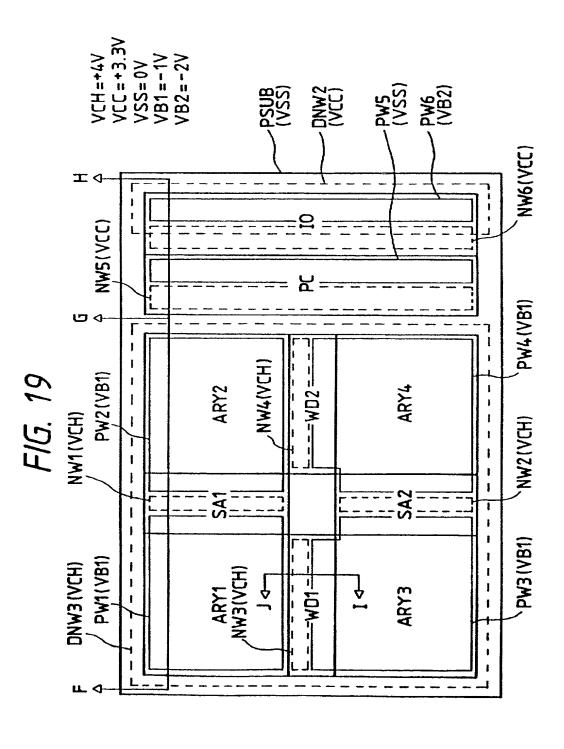


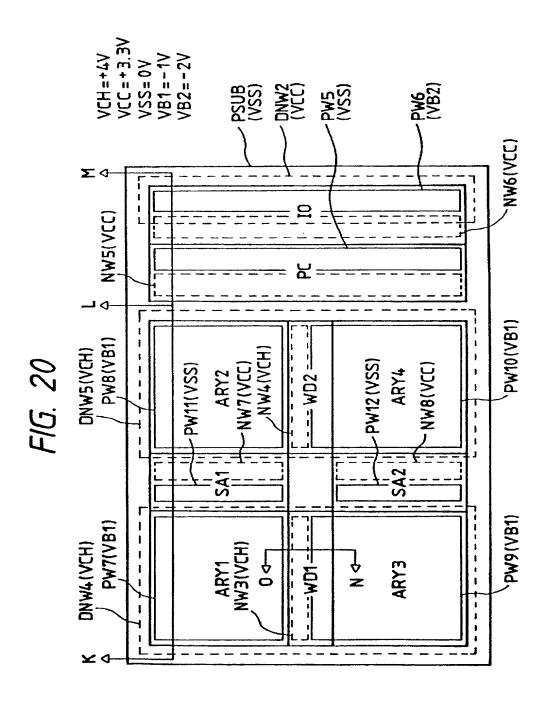
FIG. 17

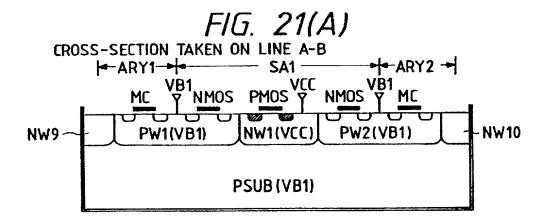


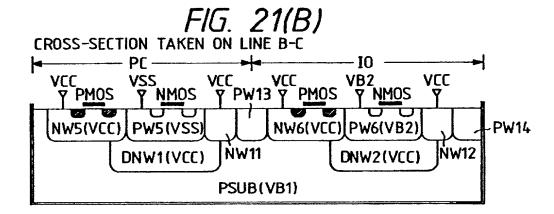
Oct. 12, 1999

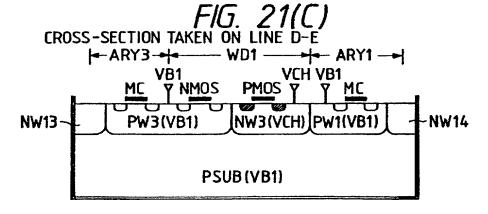






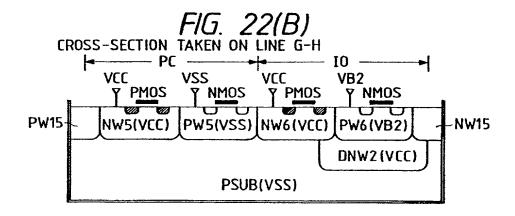


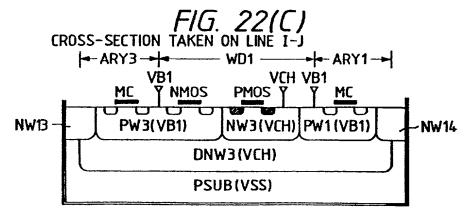




: P* DIFFUSION LAYER O: N* DIFFUSION VCH=+4V VCC=+3.3V VSS=0V VB1=-1V VBB=-2V

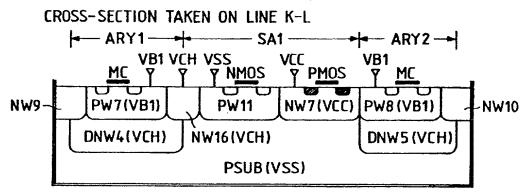
FIG. 22(A) CROSS-SECTION TAKEN ON LINE F-G - ARY1 ---SA1-ARY2-VB1 VEH VB1 PMOS Y NMOS 7 **NMOS** MC NW9 **PW1(VB1)** NW1(VCH) PW2 (VB1) NW10 DNW3(VCH) PSUB(VSS)

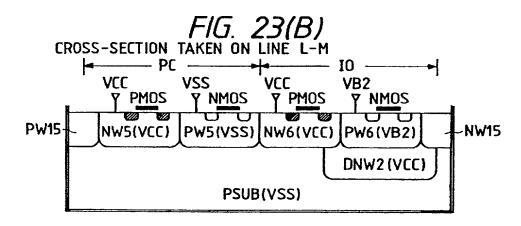


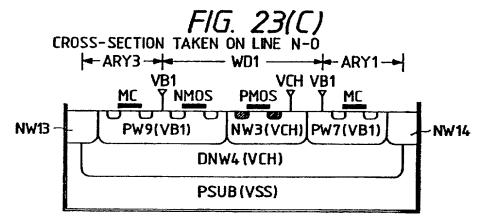


■:P* DIFFUSION □:N* DIFFUSION LAYER LAYER VCH=+4V VCC=+3.3V VSS=0V VB1=-1V VBB=-2V

FIG. 23(A)







■:P* DIFFUSION □:N* DIFFUSION LAYER LAYER VCH=+4V VCC=+3.3V VSS=0V VB1=-1V VBB=-2V